

A LOW-POWER VISION PROCESSING PLATFORM FOR MOBILE ROBOTS

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ABSTRACT

The paper proposes an implementation for a highly customizable FPGA-based vision processing module for mobile applications. The module can be directly integrated into the AMiRo mini robot to enhance the robot's vision processing capabilities while significantly reducing the CPU load. Dynamic reconfiguration can be utilized to further improve the resource utilization of the platform.

1. INTRODUCTION

Vision processing is a challenging task, especially in small mobile devices like smartphones or mini robots where the available energy limits processing power. In this paper we present a low power vision processing platform that can be embedded into the AMiRo mini robot (Figure 1), which is developed at CITEC (Center of Excellence Cognitive Interaction Technology, Bielefeld) [1]. AMiRo is a modular robot platform for research and education that combines sophisticated sensor technology with low-power processing modules at affordable cost. AMiRo is designed for soccer playing in the AMiRESoT robot soccer league. Therefore, efficient vision processing is an essential requirement for the mini robot. In order to relieve the microcontrollers inside the AMiRo from these time-consuming tasks, the proposed vision processing platform serves as a hardware accelerator or as a preprocessing engine. The platform is based on a field programmable gate array (FPGA) since the inherent parallelism of these devices can be utilized very efficiently for many vision processing algorithms [2, 3]. Furthermore, partial dynamic reconfiguration of the FPGA offers an interesting perspective to further increase the resource efficiency of the platform.

2. THE MINI ROBOT AMIRO

The cylindrical body of the robot has an outer diameter of 100 mm and contains all electronic modules for information processing and communication, the sensors and actuators as well as the power supply. Because of its modular architecture, the AMiRo can be easily configured to the user's

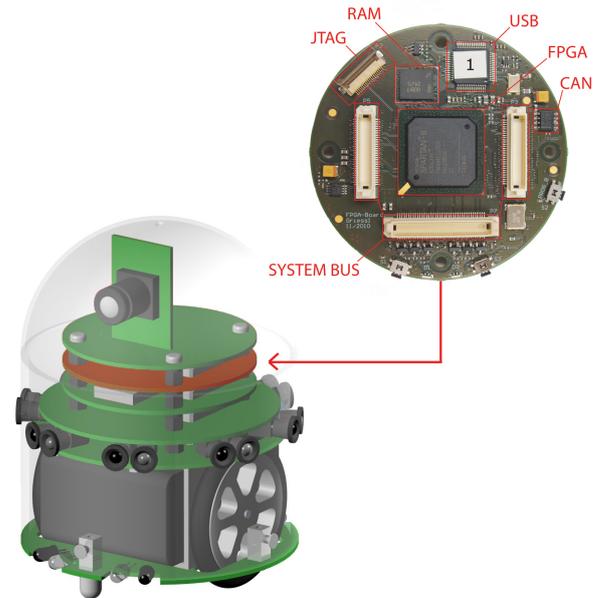


Fig. 1. The FPGA-based vision processing module is integrated into the AMiRo mini robot

actual requirements. In each configuration, a power module and an action module constitute the base system. The power module provides power management and power monitoring as well as wireless communication facilities. A low-power Cortex-M3 microcontroller on the action module implements the interface to the motor drivers and various sensors that are part of the action module, like accelerometer, gyroscope, compass, infrared proximity sensors and capacitive touch sensors. For extending the basic capabilities of the robot, additional modules can be easily integrated. Perception modules add additional sensors and cognition modules add processing power by means of additional microcontrollers, FPGAs or ASICs. For inter module communication a system bus has been defined for the AMiRo. The bus combines serial communication standards like CAN, UART, SPI and parallel protocols like camera capture interface and an external memory interface.

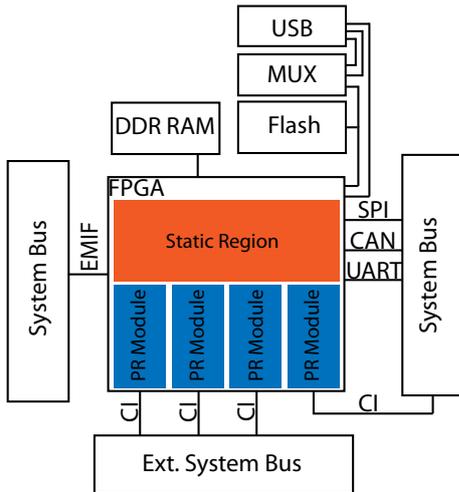


Fig. 2. Overview of the vision processing platform

3. THE PROCESSING PLATFORM

The proposed vision processing module serves as a cognition module in the AMiRo and can be directly connected to a dedicated perception module, which contains up to four camera modules, enabling stereo and omni vision. The platform consists of a PCB with a diameter of 70 mm, it is equipped with a Xilinx Spartan 6 FPGA and 1 GBit low power DDR SDRAM, which is used as an additional frame buffer. Figure 2 gives an overview of the implemented architecture. Various Xilinx Spartan 6 FPGAs with an FG484 package can be used, ranging from LX45 devices with 43,661 logic cells up to LX150 devices with 147,443 logic cells. The system bus is completely attached to the User I/Os of the FPGA and the camera capture interface is looped through the device. Therefore, the vision processing module can be efficiently utilized as a preprocessor for the captured image stream before sending it to another unit. The integrated high-speed USB device offers a transfer rate of 480 MBit/s and enables live streaming of processed data for debug purposes. Via USB a FPGA configuration can be written directly into the FPGA as well as stored in the configuration flash. Static memory can be easily extended by means of an SD-card slot on the bottom of the PCB. Energy efficiency of the module could be proven by a measured power consumption of less than 0,7 Watt for typical applications.

4. PARTIAL RECONFIGURATION

Typically, not all image processing tasks have to be executed in parallel. In this context, partial dynamic reconfiguration has important advantages for mobile robots. Depending on the current background hardware configurations can be automatically loaded into the FPGA device, i.e., one or more

hardware modules are able to process images in parallel. If a specific processing task has been finished, a new hardware configuration can be loaded to optimize the resource utilization on the fly.

The architectural design of the platform is optimized to satisfy the requirements of partial reconfiguration. In particular, the camera capture interfaces are routed to predefined regions on the FPGA. The benefit is a well-defined floorplan for partial reconfiguration, which is optimized for short wire lengths on the FPGA. As indicated in Figure 2 the FPGA resources are divided into a static region and a PR (partially reconfigurable) region [4]. No external controller hardware is required for dynamic reconfiguration. A softcore processor, located in the static region, reconfigures the PR modules inside the PR regions via the ICAP. Additionally, the processor handles the communication between the vision processing platform and the robot. In the current implementation, four PR modules are defined, which can be reconfigured separately or combined to one or two more complex modules. Reconfiguration is quite fast; depending on the used FPGA a PR module can be reconfigured in about 2 ms (LX45) or less than 7 ms (LX150).

5. CONCLUSION

The proposed FPGA-based vision processing platform can be easily utilized to analyze new algorithms and implementations. Up to four cameras can be handled in parallel and external memory is available for applications that require more memory than available in the FPGA. An optimized PCB design eases dynamic reconfiguration of the FPGA so that implementations can be exchanged at run-time depending on the current needs of the application. Two implementations are currently under development to prove the efficiency of the platform: an optical flow module and a color recognition module, which can be adapted in terms of the number of recognizable blocks and colors.

6. REFERENCES

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